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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/347,106	07/02/1999	STANLEY A. HRONIK	M-7086US	3360

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SKJERVEN MORRILL LLP
25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110

EXAMINER	
ANDERSON, MATTHEW D	

ART UNIT	PAPER NUMBER
2186	19

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/347,106	HRONIK, STANLEY A.	
	Examiner	Art Unit	
	Matthew D. Anderson	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 November 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-58* is/are pending in the application.

4a) Of the above claim(s) *56* is/are withdrawn from consideration.

5)☒ Claim(s) *38-45* is/are allowed.

6)☒ Claim(s) *1-13,17,25,27-36,46-55,57 and 58* is/are rejected.

7)☒ Claim(s) *14-16,18-24,26 and 37* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *10 November 2003* is: a)☐ approved b)☒ disapproved by the Examiner

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *17* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. In response to the amendment filed 11/10/03:

claim 56 has been canceled;

claims 1, 3-5, 28, 40, 46, 48-49, and 54 have been amended;

Drawings

2. The drawings were received on 11/10/03. These drawings are not approved because the D_{in} lines 23 and 33 in figure 2 appear to be mistakenly labeled as D_{out} lines as in the previous informal drawings.

Allowable Subject Matter

3. Claims 38-45 are allowed.

4. Claims 14-16, 18-24, 26, and 37 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is a statement of reasons for the indication of allowable subject matter: the prior art does not teach or suggest the combination of claim elements specifically including the following:

[Claim 14]: at least two registers for providing both a burst address received at the address bus and at least one read/write control signal received at the input terminal of the memory circuit to the at least two memory blocks sequentially in one clock cycle;

[Claim 18]: selecting a first write burst address stored in a first register corresponding to the last write burst operation;

[Claim 20 & 38]: the write data item is written to one of the memory blocks at the initiation of the first write burst operations, and the next write data item is written to the other one of the memory blocks half a clock cycle after the initiation of the first write burst operation;

[Claims 26 & 37]: generating an echo clock signal when a read data item is provided on the data bus.

6. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

7. Since allowable subject matter has been indicated, applicant is encouraged to submit formal drawings in response to this Office action. The early submission of formal drawings will permit the Office to review the drawings for acceptability and to resolve any informalities remaining therein before the application is passed to issue. This will avoid possible delays in the issue process.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-4, 10-13, 17, 25, 27-31, 46-54, and 57-58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ryan (US Patent # 5,749,086) and Nakamura *et al.* (A 500MHz Pipeline-Burst Cache SRAM with Point-to -Point Noise Reduction Coding I/O).

10. With respect to claims 1, 28, 46, 48, 50, 52, 54, Ryan discloses:

an address bus for receiving an address, as shown in item 105 of figure 3;

at least two memory blocks, as shown by the memory array 101 in figure 3;

an data bus for receiving data, as shown in item 130 of figure 3;

a sequential write burst and sequential read burst via the data bus, as shown in figure 19.

11. With respect to claims 2, 10, 29, 46, 49, Ryan discloses:

the first and second write data items are provided on the data bus at least one clock cycle after the first write burst operation is initiated, by teaching in figure 15, idle states (NOP) occurring after the write mode is selected, but before the write burst is started;

the first and second read data items are provided on the data bus at least one clock cycle after the first read burst operation is initiated, by teaching in figure 7, idle states (NOP) occurring after the read mode is selected, but before the read burst is started.

12. With respect to claims 3, 30, 48, 52, Ryan discloses a read/write control signal for indicating a write burst or a read burst operation, by teaching in Table 1 of column 6, lines 35-40, determining the mode by the command signals.

13. With respect to claims 4, 31, Ryan discloses second and third read or write bursts, as shown in figure 19.

14. With respect to claim 11, Ryan discloses an output circuit enable, by teaching in figure 19 of an output enable signal.

15. With respect to claim 12, Ryan discloses:

an input terminal for receiving the control signals, by showing the command decode device (104) in figure 3;

the output circuit being enabled by a 3-state signal, by teaching in Table 2 of column 6, lines 50-60, determining the read and write modes by the command signals.

16. With respect to claims 13, 47, 51, Ryan discloses a multiplexer for receiving a clock signal and read data items, and sequentially transferring to an output bus of the multiplexer, the read data items in accordance with the state of the clock signal, as shown in figures 3 and 19.

17. With respect to claims 25, 53, Ryan discloses a SRAM, in column 11, line 20.

18. With respect to claim 27, Ryan discloses:

a data-in bus for receiving write data items, as shown by the bus connected to the data-in buffer (126) of figure 3;

a data-out bus for providing read data items, as shown by the bus connected to the data-out buffer (128) of figure 3.

19. With respect to claims 54 and 57-58, Ryan discloses that consecutive read and write burst operations are capable to be performed sequentially in any order, by teaching in figure 11 of a burst read followed by a write, and in figure 19, of a burst write followed by a read.

20. With respect to the independent claims 1, 28, and 54, Ryan teaches all other claim limitations, but does not specifically disclose initiating a read/write burst on the next consecutive clock cycle after the initiation of the first write/read burst. Nakamura et al. disclose in figure 1, of a Read burst signal and Read burst data directly following Write burst signal and write burst data respectively, with no dead cycles there between.

21. With respect to claim 46, Nakamura et al. disclose providing read data on the data bus within one clock cycle after the read operation is initiated and reading the first data item overlap the reading of the second data item, by showing in figure 1 that the reading of item 30-33 occur in the I-cycle immediately after the command at T24, while the reading of item 31 and 32 share I-cycle beginning at T32.

22. It would have been obvious to one of ordinary skill in the art, having the teachings of Ryan and Nakamura et al. before him at the time the invention was made, to modify the memory system with read and write bursts of Ryan, to include the consecutive initiation of the burst cycles, as in the memory access control system with read and write bursts of Nakamura et al., in order to completely eliminate idle clock cycles on the data bus, as taught by Nakamura et al. in column 1 of page 406.

23. Claims 5-9, 32-36, and 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ryan, Nakamura et al., and Hayes et al. (US Patent # 5,987,570).

24. Ryan and Nakamura et al. teach all other limitations of the parent claims, but does not specifically disclose the following:

25. With respect to claims 5, 32, 55, Hayes et al. disclose overlapping of the transfer of data items during half a clock cycle, by teaching in column 5, lines 12-15, overlapping of the first and second read block transactions.

26. With respect to claims 6-7, 17, 33-34, Hayes et al. disclose overlapping of write bursts, by teaching in column 14, lines 4-5, overlapping a write to physical memory with another burst.

27. With respect to claims 8-9, 35-36, Hayes et al. disclose overlapping of read bursts, by teaching in column 5, lines 12-15, overlapping of the first and second read block transactions.

28. It would have been obvious to one of ordinary skill in the art, having the teachings of Ryan, Nakamura et al., and Hayes et al. before him at the time the invention was made, to modify the memory system with read and write bursts of Ryan and Nakamura et al., to include overlapping of memory read/writes, as in the memory access control system of Hayes et al., in order to improve system throughput, as taught by Hayes et al..

Response to Arguments

29. Applicant's arguments with respect to claims 1-58 have been considered but are moot in view of the new ground(s) of rejection.

30. With respect to claim 46, although the reading of the data items do not occur in parallel, they share the same I-cycle. The *Microsoft Bookshelf Dictionary* defines "overlap" as "To have

an area or a range in common with." Since the readings of these data items occur in the common I-cycle beginning at T32, they can be said to overlap. The Examiner recommends amending the claim language to be similar to that of the half clock cycle in claim 8

Conclusion

31. Applicant's submission of an information disclosure statement under 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p) on 11/10/03 prompted the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 609(B)(2)(i). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

32. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew D. Anderson whose telephone number is (703) 306-5931. The examiner can normally be reached on Monday-Friday, 2nd Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on (703) 305-3821. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Matthew D. Anderson
December 5, 2003

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100